

University of St. Thomas ENGR 230 ---- Digital Design

Fall 2009	4 Credit Course Monday, Wednesday, Friday from 1:35 p.m. to 2:40 p.m. Lecture: Room OWS 275 Lab: Section 51: OSS LL14 Tuesday from 1:30-4:30 Section 52: OSS LL14 Thursday from 1:30-4:30 Section 53: OSS LL14 Thursday from 5:30-8:30 Section 54: OSS LL14 Wednesday from 5:30-8:30
Instructor(s)	Dr. Christopher S. Greene Phone: (651) 962-5768 Office: OSS109 E-Mail: csgreene@stthomas.edu Lab Section 51: Ian Tran E-Mail: tran0500@stthomas.edu Lab Section 52: Ian Tran E-Mail: tran0500@stthomas.edu Lab Section 53: Attila Magyar E-Mail: magy0108@stthomas.edu Lab Section 54: Keith Berrier E-Mail: berrier@StThomas.edu
Required Text	“Digital Design – Principles and Practices”, 4 th ed., John Wakerly, Prentice Hall. ISBN 0-13-186389-4
Optional Texts	“Digital Design”, 3 rd ed., Mano, Prentice Hall Guide for Lab Reports: “Pocket Book of Technical Writing for Engineers and Scientists”, Leo Finkelstein, Jr., McGraw-Hill. “VHDL For Digital Design”, Frank Vahid, Wiley. ISBN 13-978-0-470- 05263-1. USB Flash Drive (used in Lab). At least 256K for use in this class.
Course Description	Introduction to the design of digital logic. Topics include Boolean logic, design and optimization of combinational and sequential logic, the use of programmable logic devices, logic hazards, electronic implementation of logic gates. Students will be expected to specify, design, simulate, construct and test digital circuits and document all phases of the process.
Class Web page	This class will use Blackboard. See http://blackboard.stthomas.edu/ for all class communication.
Prerequisites	None.

ENGR 230 — Digital Design

Disability Accommodation	Students with disabilities who may need accommodations in this class are encouraged to contact the Enhancement Program - Disability Services at 651-962-6315 as soon as possible. See http://www.stthomas.edu/enhancementprog/ for more information.
Academic Integrity	All students are expected to understand and follow the University of St. Thomas policies on Academic Integrity. These are described at: http://www.stthomas.edu/policies/student_policy_book/Academic_rights_and_procedures.asp
Attendance	Students are expected to attend all class sessions. All absences require that the instructor be informed in advance if at all possible. Circumstances that prevent attendance will be honored up to two instances. Contact the instructor when a special situation arises.
Absence for Flu	Because of the possibility of a flu pandemic, I will be particularly understanding of absences due to the flu. Student's responsibilities are: <ol style="list-style-type: none">1) If you have flu symptoms (fever and sore throat) stay home and self-isolate. <u>Notify all your professors ASAP.</u>2) Stay isolated until you have been fever-free for at least 24 hours.3) You are still responsible for the material. If I know you have the flu, I will work hard to put the notes on Blackboard. Keep up using Blackboard and use email to ask any questions. See me when you have recovered. If you have notified me in a timely manner and have been diligent about keeping up, I will be understanding of needing more time for assignments, including exams.4) Don't attend lab until you have recovered. You can make up the work later. If necessary, this can be during J-term.5) If I get sick, I will use Blackboard to communicate with you our plan for continuing the course. Come to class as usual unless I email/blackboard you otherwise.6) Please don't abuse this. Getting the flu twice is unlikely and if everyone gets the flu the morning of an exam.... <u>I will treat you as professionals as long as you act as professionals.</u>

ENGR 230 — Digital Design

Objectives for ENGR 230

(letters in parentheses refer to EE program outcomes)

Learning Objectives

1. Understanding of the principles of combinational and sequential logic design as demonstrated in quizzes and tests. (a, ee)
2. Ability to apply those principles to the design and analysis of practical digital systems as demonstrated in laboratory experiments and student design projects. (b, c, e)
3. Ability to use software tools and lab instruments to design, simulate, implement, test and document digital systems using 74xx as well as programmable components. (k)

Skills

Upon successful completion of the course, the student will be able to:

1. Use mixed signal scopes for debugging digital circuits, (k)
2. Translate numbers between binary, decimal and hexadecimal codes, (a, ee)
3. Perform arithmetic on binary, octal, and hexadecimal numbers, (a, ee)
4. Convert between schematics, truth tables, and Boolean equations, (a)
5. Determine equality of Boolean expressions, (a, ee)
6. Simplify Boolean expressions, (a, ee)
7. Design combinational logic circuits to accomplish specified tasks, (b)
8. Design sequential logic circuits to accomplish specified tasks, (b)
9. Use VHDL to synthesize combinational and sequential circuits, (b, k)
10. Document digital designs sufficiently for others to use them (g)
11. Verify the performance of a digital design using software simulation tools, (b, k)
12. Analyze circuits to detect and remove hazards, and (a)

Knowledge

Upon successful completion of the course, the student will be able to explain:

1. How binary codes are used to represent characters, pictures, and numbers, (a, ee)
2. The advantages of 2s complement, binary coded decimal, and gray codes, (a, ee)
3. Boolean algebra and logic gate behavior, (a, ee)
4. Function and application of common MSI components, (a)
5. Flip Flop construction and behavior in terms of combinational logic, (a)
6. Metastability and how synchronizers work, (a)
7. Architectures, capabilities and prices of current programmable devices, (a)
8. Implementation issues including fan-out, noise, power, and speed. (a)

Attitudes

During the course, the student must at all times exhibit:

1. Concern for the safety of themselves and others, (f)
2. Efficient use of time and resources, (f)
3. Courtesy to classmates, faculty and staff, (f)
4. Personal integrity, (f)
5. Desire for clear communication, (g)
6. Desire to achieve objectives. (f)

ENGR 230 — Digital Design

Schedule as of August 1, 2009

<u>Date</u>	<u>Chapter</u>	<u>Topic</u>	<u>Lab</u>	<u>Quiz</u>
Sept 9	1	Course Introduction and Tools	#1 -Tools of the Trade	
Sept 11	2	Number Systems and Codes		
Sept 14	2	Binary arithmetic		
Sept 16	2	Binary arithmetic continued		#1
Sept 18	4.1-2	Boolean Algebra		
Sept 21	4.1-2	Combinational Circuit Analysis		
Sept 23	4.3-4	Combinational Circuit Synthesis	#2 – LSI Gates	#2
Sept 25	4.3-4	Combinational Circuit Synthesis		
Sept 28	4.3-6, 5.3	Combinatorial Circuit Synthesis Review and Intro to PLD's		
Sept 30	5.3	Introduction to VHDL	#2B – Intro to PLD's	#3
Oct 2	5.3	More VHDL		
Oct 5	6	Documentation of Digital Logic – Block Diagrams, Logic diagrams and Schematics		
Oct 7	6.1-2	Documentation – timing diagrams and HDL listings	#3 – Intro to Xilinx	#4
Oct 9	6.4-6.5	Decoders		
Oct 12	6.6-6.9	Multiplexers, Demultiplexers and Tri-state Buffers		
Oct 14	6.10-11, 9.1	ALUs and ROMs		
Oct 16		Combinational Review		Exam 1
Oct 19		Combinational Review		
Oct 21	7.1-3	Latches and Flip Flops	#4 – Modular Design	
Oct 23	7.12	Sequential PALs		
Oct 26	7.4-10	Timing Diagrams and sequential Circuits		
Oct 28		Sequential circuit analysis	#5 – ALU	#5
Oct 30		Mid-term break – grades due		
Nov 2	8	Sequential circuit design		
Nov 4	9	Sequential VHDL, counters and		#6

ENGR 230 — Digital Design

		shift registers		
Nov 6	9	System design techniques		
Nov 9	9	State machines		
Nov 11	9	PLD based state machines	#6 – Latches and FFs	
Nov 13		Sequential Review		
Nov 16	9	Sequential Review		Exam 2
Nov 18	9	Sequential Design Example – Serial to Parallel Conversion	#7 – Design of Sequential circuits	
Nov 20	9	Sequential Design Example – Multiplier		
Nov 23	8.8,8.9	Metastability and Synchronizers		
Nov 25	8.8,8.9	Metastability and Synchronizers		#7
Nov 27		Thanksgiving Holiday		
Nov 30	9	Memory Devices		
Dec 2	9.5	CPLDs and FPGAs		
Dec 4	9.6	CPLDs and FPGAs		
Dec 7		A-D and D-A		
Dec 9		Review		#8
Dec 11		Review /How IC's are made.		Final I
Dec 16		Final		Final II

Special Thanks to BPM Microsystems for supplying our department with a [Device Programmer](#). See their latest breakthrough in flash device programming technology - [Flashstream: High-Speed Flash Memory Programming Leader](#).

ENGR 230 – Digital Design Laboratory Descriptions

1. Tools of the Trade: An introduction to lab instruments commonly used in electrical engineering. Learn to use the oscilloscope, signal generator, power supply and multimeter. (2 weeks)
2. Basic Logic Gates: Learn to use basic logic gates (AND, OR, NOT) in common 74xx packages, and build simple logic circuits. Digital like your granddad did it. (1 week)
- 2b. You will then have the opportunity to do the same simple logic circuit using a PLD. Digital the modern way. (1 week)
3. Simple Combinational Design in VHDL: Implementing combinational circuits in an FPGA.
4. Divide and Conquer: Modular design in digital systems. Multiplexers and decoders.
5. ALU Design in VHDL: Design a circuit to add and subtract as well as shift, and, or and negate. The first step towards your own computer.
6. Flip Flops and Latches: Build memory elements from combinational logic gates
7. Sequential Design in VHDL: Project!

All students are expected to complete lab 7.

Grading Policy

In this course, your assessment of your own ability contributes to the grade. Below is the way this is done.

Learning Objectives for this course and criteria for A, B, C, and D level performance are provided below. To achieve a passing grade, students are required to present documentation to the instructor that demonstrates accomplishment of the learning objectives at the desired performance level. An example of documentation for one objective might read as follows:

“Skill 3 - Perform arithmetic on binary, octal, and hexadecimal numbers. This is demonstrated at an acceptable level in quiz 1 and problem 5 of exam 1. But it is demonstrated at a good level in lab reports 5 and 9.”

Quizzes, exams, homework, and lab reports cited must be included in the grading documentation packet. If students wish to use other projects for documentation, they should consult with the instructor to ensure that the project will provide adequate documentation. The midterm grading documentation packet is due on 25 October and the final grading documentation packet is due on 16 December.

Grading Rubric for an individual piece of evidence such as an exam problem, or report

Good: Demonstrates an accomplishment of the learning objective with a sufficient mastery to be able to solve typical problems encountered by engineers.

Good But...: Demonstrates an accomplishment of the learning objective with some mastery but short of that needed to solve typical problems encountered by engineers.

Acceptable: Demonstrates through tangible evidence an accomplishment of a learning objective at a minimal level that shows they might work in the field under appropriate supervision, but did not demonstrate sufficient mastery of the subject for the instructor to be confident of the student's ability to solve problems independently.

Not Acceptable: Does not demonstrate accomplishment of the learning objective.

Overall Course Grade

A: Demonstrates through tangible evidence a mastery of course material to the extent that the student can apply the knowledge gained in the class to solve problems in the subject area beyond those solved in class.

B: Demonstrates through tangible evidence an accomplishment of all learning objectives with a sufficient mastery to be able to solve typical problems encountered by engineers in

ENGR 230 — Digital Design

the subject matter of the course. However, the student has not demonstrated the ability to apply the knowledge gained in the course to problems beyond those solved in class

C: Demonstrates through tangible evidence an accomplishment of all learning objectives at a minimal level that shows they might work in the field under appropriate supervision, but did not demonstrate sufficient mastery of the subject for the instructor to be confident of the student's ability to solve problems independently.

D: Does not demonstrate accomplishment of all learning objectives specified in the syllabus. However, student shows evidence that they learned enough from the course that it should count for college credit. This grade indicates that the student has not demonstrated mastery of the material at the level needed to continue in classes that have this course as a prerequisite.

F: Does not provide evidence of sufficient learning to receive college credit for this course.

Typing Course Grade to objectives

A	Consistent good work in all objectives
A-	Consistent good work in most objectives, occasional good work in all
B+	Consistent good work in some objectives, occasional good work in all
B	Occasional good work in all objectives
B-	Occasional good work in most objectives, acceptable work in all
C+	Occasional good work in some objectives, acceptable in all
C	Acceptable work in all objectives
C-	Unacceptable work in some objectives, with strong evidence of improvement
D+	Unacceptable work in some objectives, with evidence of improvement
D	Unacceptable work in some objective
D-	Unacceptable work in many objectives
F	Unacceptable work in most objectives